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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/424,966	03/06/2000	AKIHIDE SHIBATA	247322001700	8894

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EXAMINER	
LOKE, STEVEN HO YIN	
ART UNIT	**PAPER NUMBER**
2811	

DATE MAILED: 09/24/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)
	09/424,966	SHIBATA ET AL.
	Examiner	Art Unit
	Steven Loke	2811

-- The MAILING DATE of this communication appears on the cov r sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *05 May 2003 and 08 August 2003* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-36* is/are pending in the application.

4a) Of the above claim(s) *4,5,7,9,11,13,15,17,19,21,23,25,27 and 29-36* is/are withdrawn from consideration.

5)☒ Claim(s) *10,12,16,18,20 and 26* is/are allowed.

6)☒ Claim(s) *1-3,6,8,14,22,24 and 28* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other:

1. Claim 22 is objected to because of the following informalities: lines 8-9, the phrase "...is connected to substrate terminal..." is not understood. It is believed that the phrase should read as "...is connected to a substrate terminal...". Appropriate correction is required.

2. Claims 22, 24 and 28 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Claim 22, lines 10-11, the phrase "a gate terminal of said P-type semiconductor element is connected to a substrate terminal of said N-type semiconductor element are connected to each other" is not understood. It is believed that the phrase should read as "a gate terminal of said P-type semiconductor element is connected to a substrate terminal of said N-type semiconductor element".

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. Claims 1-3, 6, 8 and 14 are rejected under 35 U.S.C. 103(a) as being unpatentable over Chang et al. in view of Iwamatsu.

In regards to claim 1, Chang et al. disclose a CMOS in fig. 1l. It comprises: a semiconductor device comprising a plurality of semiconductor elements, each being provided with a source region [26, 34] and a drain region [23, 32] in a well [8, 12] formed in a semiconductor layer, and a gate terminal [20', 20''] fabricated on a channel region,

the channel region is formed between the source region and drain region, a gate terminal formed on a gate insulating film [16, 18], wherein: each of the semiconductor elements is electrically separated from the others; and the well in each of the semiconductor elements is provided with a substrate terminal region [28, 30] with a contact hole formed on it; regions [28, 30] are formed at regions other than the source region and drain region.

Chang et al. differ from the claimed invention by not showing a source terminal, a drain terminal and a substrate terminal in each of the semiconductor elements. In addition, Chang et al. further differ from the claimed invention by not showing each gate terminal receives a first input signal and each well receives a second input signal, and the first and second input signals are different signals that are synchronized with each other.

Iwamatsu shows a source terminal, a drain terminal and a substrate terminal in each of the semiconductor elements (PMOS and NMOS) in fig. 2. In addition, Iwamatsu further shows each gate terminal [5] receives a first input signal and each well [2, 3] receives a second input signal [V_{BG2}, V_{BG1}] in figs. 1-4. Fig. 4 shows the first input signal (V_{IN} is about 2.5 V) and the second input signals (V_{BG1} = V_{BG2} = CLK1 = CLK2 = 0 volt) are different signals that are synchronized with each other at a time interval.

Since both Chang et al. and Iwamatsu teach a CMOS structure with well contact regions for well voltages, it would have been obvious to have a source terminal, a drain terminal and a substrate terminal in each of the semiconductor elements of Iwamatsu in Chang et al. because they provide electrical connection between the semiconductor

elements and the external circuit. It would also have been obvious to have the electrical connections of Iwamatsu in Chang et al. because they create a CMOS level shifter circuit having a concise level shift and a low reduction in an integration degree. In addition, the electrical insulation layer [14] of Chang et al. insulates all the terminals of the PMOS, NMOS and the wells.

In regards to claim 2, the combined device inherently discloses the operating characteristics are changed by adjusting impurity concentration in the channel region and levels of a high voltage and a low voltage applied to the gate terminal and substrate terminal.

In regards to claim 3, the combined device of Chang et al. and Iwamatsu shows the semiconductor layer in each of the semiconductor elements is electrically separated from each other by means of an oxide film [14 of Chang et al.].

In regards to claim 6, Chang et al. differ from the claimed invention by not showing a high potential is supplied to a source terminal of the PMOS and a low potential is supplied to a source terminal of the NMOS, the gate terminals of the PMOS and NMOS are connected to each other to form a first input terminal, the substrate terminals of the PMOS and NMOS are connected to each other to form a second input terminal, and the drain terminals of the PMOS and NMOS are connected to each other to form an output terminal.

Iwamatsu shows showing a high potential V_{DD} is supplied to a source terminal of the PMOS and a low potential (ground) is supplied to a source terminal of the NMOS, the gate terminals of the PMOS and NMOS are connected to each other to form a first input

terminal V_{in}, the substrate terminals of the PMOS and NMOS are connected to each other to form a second input terminal when the clock voltages are 0 volt (CLK1=CLK2=0 volt), and the drain terminals of the PMOS and NMOS are connected to each other to form an output terminal V_{out} in figs. 1-4.

Since both Chang et al. and Iwamatsu teach a CMOS device, it would have been obvious to have the circuit connections and potentials of Iwamatsu in Chang et al. because they provide a CMOS level shifter circuit having a concise level shift and having a low reduction in an integration degree. In addition, the semiconductor structure of Chang et al. can support any desired CMOS wiring connections.

In regards to claim 8, Chang et al. and Iwamatsu differ from the claimed invention by not showing the claimed threshold voltage of each of the P-type semiconductor element and N-type semiconductor element.

It would have been obvious to have the threshold voltage of claim 8 because it depends on the impurity concentrations of the wells and the voltage applied to the second input terminal.

In regards to claim 14, Chang et al. and Iwamatsu differ from the claimed invention by not showing the claimed threshold voltage of each of the P-type semiconductor element and N-type semiconductor element.

It would have been obvious to have the threshold voltage of claim 14 because it depends on the impurity concentrations of the wells and the voltage applied to the second input terminal.

5. Applicant's arguments filed 5/5/03 have been fully considered but they are not persuasive.

It is urged, in pages 12-13 of the remarks, that the Examiner appears to alleging that the one second input signal (received at one substrate terminal) is synchronized with a different second input signal (received at a second substrate terminal). However, as mentioned in the rejection, each gate terminal [5] receives a first input signal and each well [2, 3] receives a second input signal [V_{BG2}, V_{BG1}]. Fig. 4 further shows the first input signal (V_{IN} is about 2.5 V) and the second input signals (V_{BG1} = V_{BG2} = CLK1 = CLK2 = 0 volt) are different signals that are synchronized with each other at a time interval. Therefore, Iwamatsu does show all the relationship between a first input signal (received by a gate terminal fabricated on a channel region) and second input signals received at substrate terminals.

It is urged, in page 13 of the remarks, that two disclosures "teach" the same general type of device is not proper motivation to combine the devices. However, it is well known in the art that the semiconductor structure of Chang et al. is a well known CMOS device structure. The CMOS structure of Chang et al. can be used in any circuit that would require a CMOS device. Therefore, the CMOS structure of Chang et al. can be used in any circuit connection, including the circuit connection of Iwamatsu. Therefore, it is reasonable to combine the devices of Chang et al. and Iwamatsu.

6. Claims 10, 12, 16, 18, 20 and 26 are allowed.

7. Claim 22 would be allowable if rewritten to overcome the objection and the rejection(s) under 35 U.S.C. 112, second paragraph, set forth in this Office action and to include all of the limitations of the base claim and any intervening claims.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Steven Loke whose telephone number is (703) 308-4920. The examiner can normally be reached on 7:50 am to 5:20 pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Tom Thomas can be reached on (703) 308-2772. The fax phone number for the organization where this application or proceeding is assigned is (703) 872-9306.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 308-0956.

sl
September 21, 2003

Steven Loke
Primary Examiner
Steven Loke